

Structure Silicon monolithic Integrated circuit
Product Clock Generator
Type **BU2394KN**
Feature To generate clocks for digital still camera system
 Connecting a crystal oscillator generates multiple clock signals with a built-in PLL.

○ **Absolute Maximum Ratings (Ta=25°C)**

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.5 ~ 7.0	V
Input Voltage	VIN	-0.5 ~ VDD+0.5	V
Storage Temperature range	Tstg	-30 ~ 125	°C
Power dissipation	PD	530 ^{*1}	mW

- ^{*1} A measure value at mounting on 50×50×1.6mm glass epoxy substrate.
 In the case of exceeding Ta=25°C, 5.3mW should be reduced per 1°C.
- * The radiation-resistance design is not carried out.
- * Operation is not guaranteed.

○ **Operating Conditions (Ta=-5°C~+70°C)**

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	VDD	3.0	3.3	3.6	V
Input "H" Voltage	VIH	0.8VDD	-	VDD	V
Input "L" Voltage	VIL	0.0	-	0.2VDD	V
Output load	CL	0	-	15	pF

Application example

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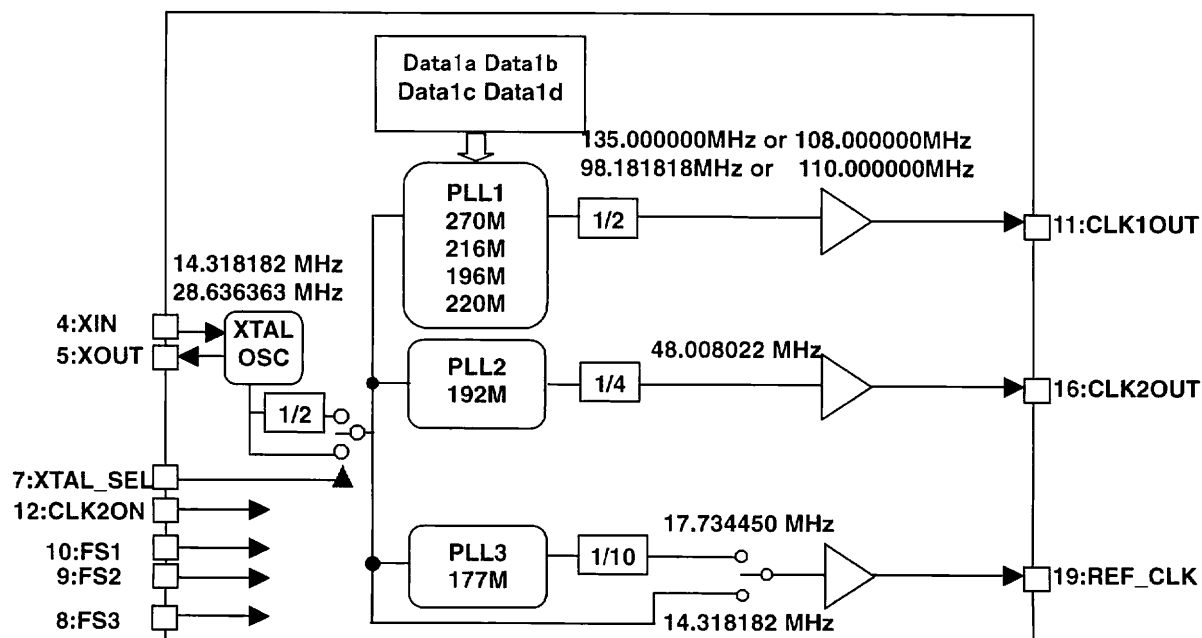
○Electrical Characteristics

(VDD=3.3V,Ta=25°C,at No Load ,unless otherwise specified)

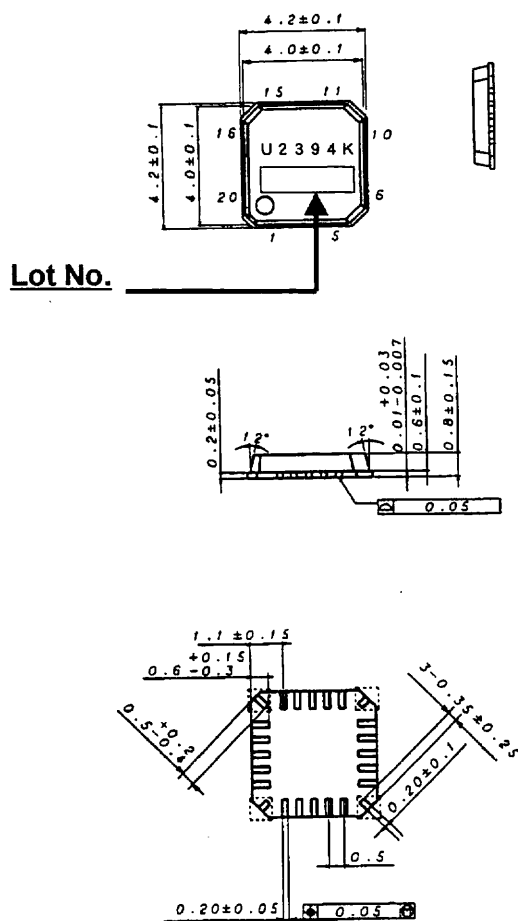
XTAL_SEL=H with crystal oscillator at a frequency of 28.636363 MHz, while XTAL_SEL=L at 14.318182 MHz

Parameter	Symbol	Limit			Unit	Conditions	
		Min.	Typ.	Max.			
Action circuit current	IDD	—	45	60	mA	At no load	
Output H voltage	CLK1	VOH1	VDD-0.5	VDD-0.2	—	V	When current load = -9.0mA
	CLK2	VOH2	VDD-0.5	VDD-0.2	—	V	When current load = -7.0mA
REF_CLK	VOHR	VDD-0.5	VDD-0.2	—	V	When current load = -4.5mA	
Output L voltage	CLK1	VOL1	—	0.2	0.5	V	When current load = 11mA
	CLK2	VOL2	—	0.2	0.5	V	When current load = 9.0mA
REF_CLK	VOLR	—	0.2	0.5	V	When current load = 5.5mA	
Pull-Up resistance value FS1,FS2,FS3,CLK2ON ,XTAL_SEL	Pullup-R	125	250	375	KΩ	Specified by a current value running when a voltage of 0V is applied to a measuring pin. (R=VDD/I)	
Output frequency							
CLK1	FS2:H FS3:H	Fclk1-1		135.000000		MHz	Xtal * (1188/63)/2
	FS2:H FS3:L	Fclk1-2		108.000000		MHz	Xtal * (1056/70)/2
	FS2:L FS3:L	Fclk1-3		98.181818		MHz	Xtal * (864/63)/2
	FS2:L FS3:H	Fclk1-4		110.000000		MHz	Xtal * (968/63)/2
CLK2	FS2,3 : HL LH HH	Fclk2-2		48.008022		MHz	Xtal * (228/17)/4
	REFCLK FS1:H	Fref1-1		14.318182		MHz	XTAL Output
	FS1:L	Fref1-2		17.734450		MHz	Xtal * (706/57)/10
Duty1 at 100MHz以下	Duty1	45	50	55	%	Measured at a voltage of 1/2 of VDD	
Duty2 at 100MHz以上	Duty2		50		%	Measured at a voltage of 1/2 of VDD	
Rise time	tr		2.5		nsec	Period of transition time required for the output to reach 80% from 20% of VDD.	
Fall time	tf		2.5		nsec	Period of transition time required for the output to reach 20% from 80% of VDD.	
Period jitter 1σ	P-J1σ		30		psec		
Period Jitter MIN-MAX	P-J MINMAX		180		psec		
Output Lock-Time	Tlock			1	msec		

○Block diagram



○Package outline, Appearance of Marker ○Pin function



VQFN-20 (Unit:mm)

Pin No.	PIN NAME	Function
1	AVDD	Analog power source
2	AVDD	Analog power source
3	AVSS	Analog GND
4	XIN	Crystal IN
5	XOUT	Crystal OUT
6	TEST1	TEST pin, normally open, equipped with pull-down
7	XTAL_SEL	Crystal oscillator selection, H:28.636 MHz, L: 14.318 MHz, equipped with pull-up
8	FS3	CLK1,2 output selection, equipped with pull-up
9	FS2	CLK1,2 output selection, equipped with pull-up
10	FS1	REFCLK output selection, equipped with pull-up
11	CLK1OUT	110M/98M/108M/135M output
12	CLK2ON	CLK2 output control, H: Enable, L: Disable, equipped with pull-up
13	VSS1	CLK1/CLK2 & Internal digital GND
14	VDD1	CLK1/2 & Internal digital power supply
15	VDD1	CLK1/2 & Internal digital power supply
16	CLK2OUT	48M output
17	VSS2	REFCLK GND
18	VDD2	REFCLK power supply
19	REF_CLK	14.3M/17.7M output
20	TEST2	TEST pin, normally open, equipped with pull-down

●Cautions on use (BU2394KN)

Basically, mount ICs to the printed circuit board for use. (If the ICs are not mounted to the printed circuit board, the characteristics of ICs may not be fully demonstrated.)

Mount 0.1μFs as bypass capacitors in the vicinity of the IC pins between 1&2 PIN and 3PIN, 13PIN and 14&15PIN, and 17PIN and 18PIN, respectively.

● Cautions on use (common)

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.

Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(1 0) Ground wiring pattern

If small-signal GND and large-current GND are provided, it will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(1 1) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

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